

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 2

FIG. 2

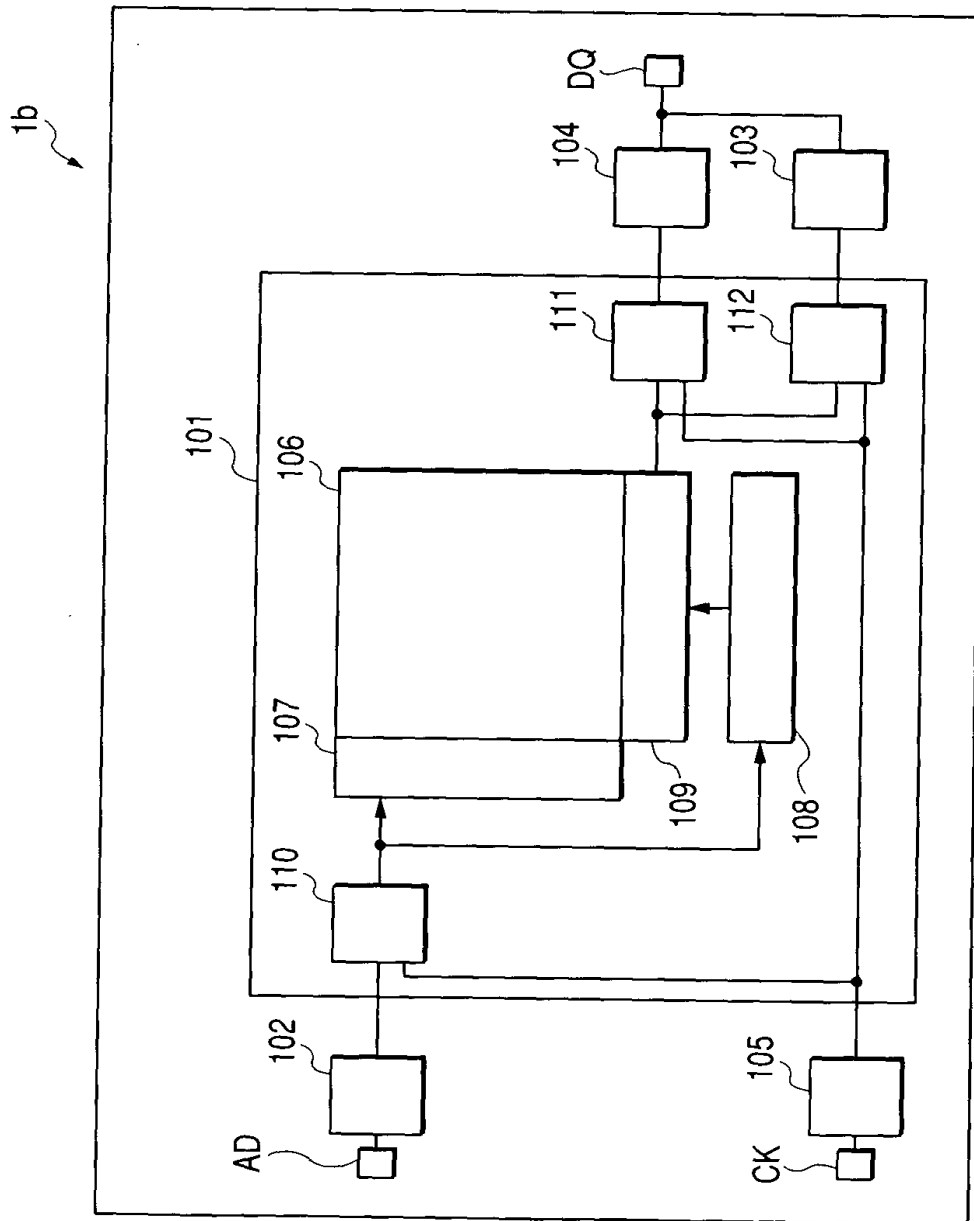


FIG. 3

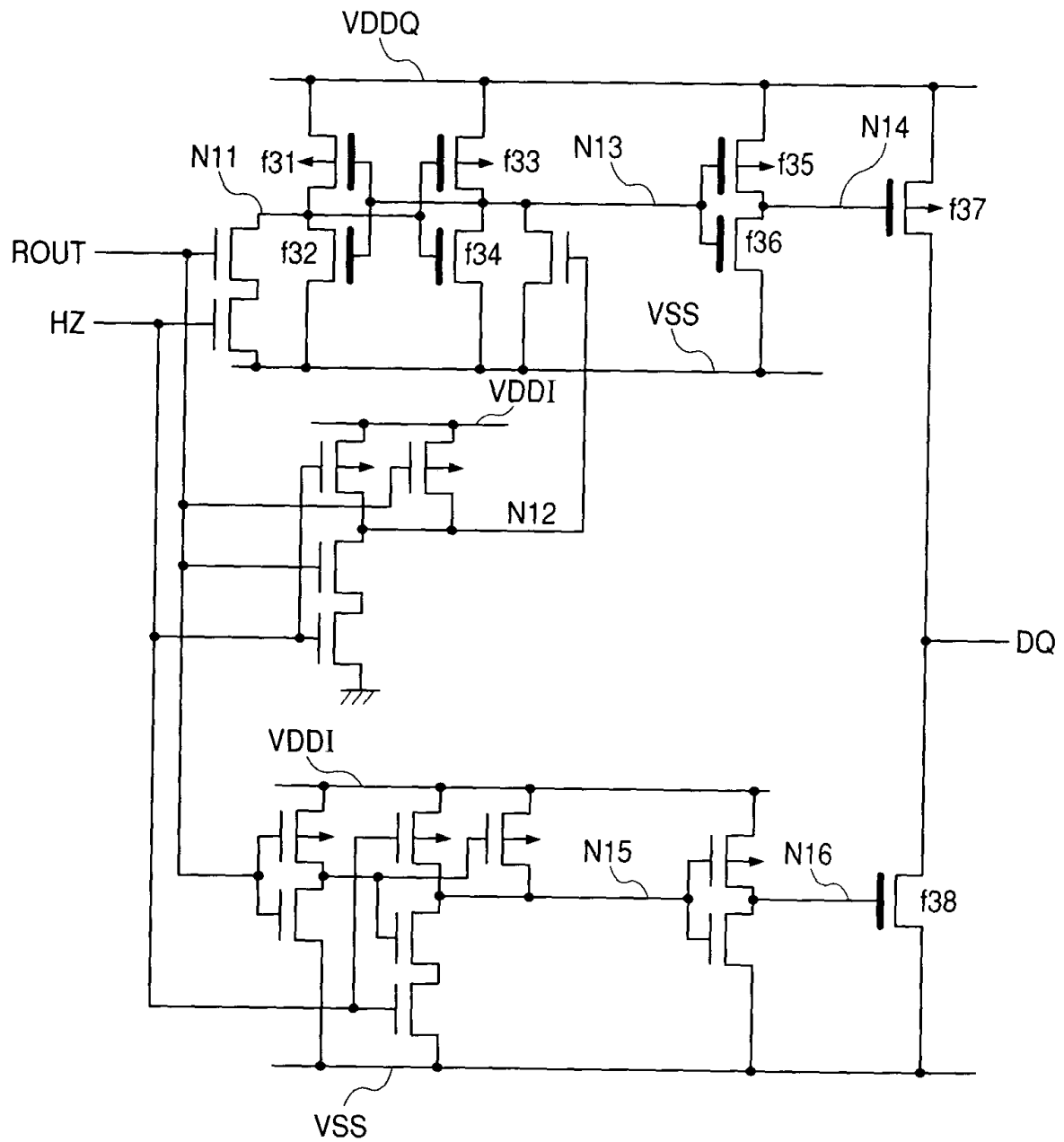


FIG. 3

APPROVED	O.G. FIG.	
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FIG. 4

FIG. 4

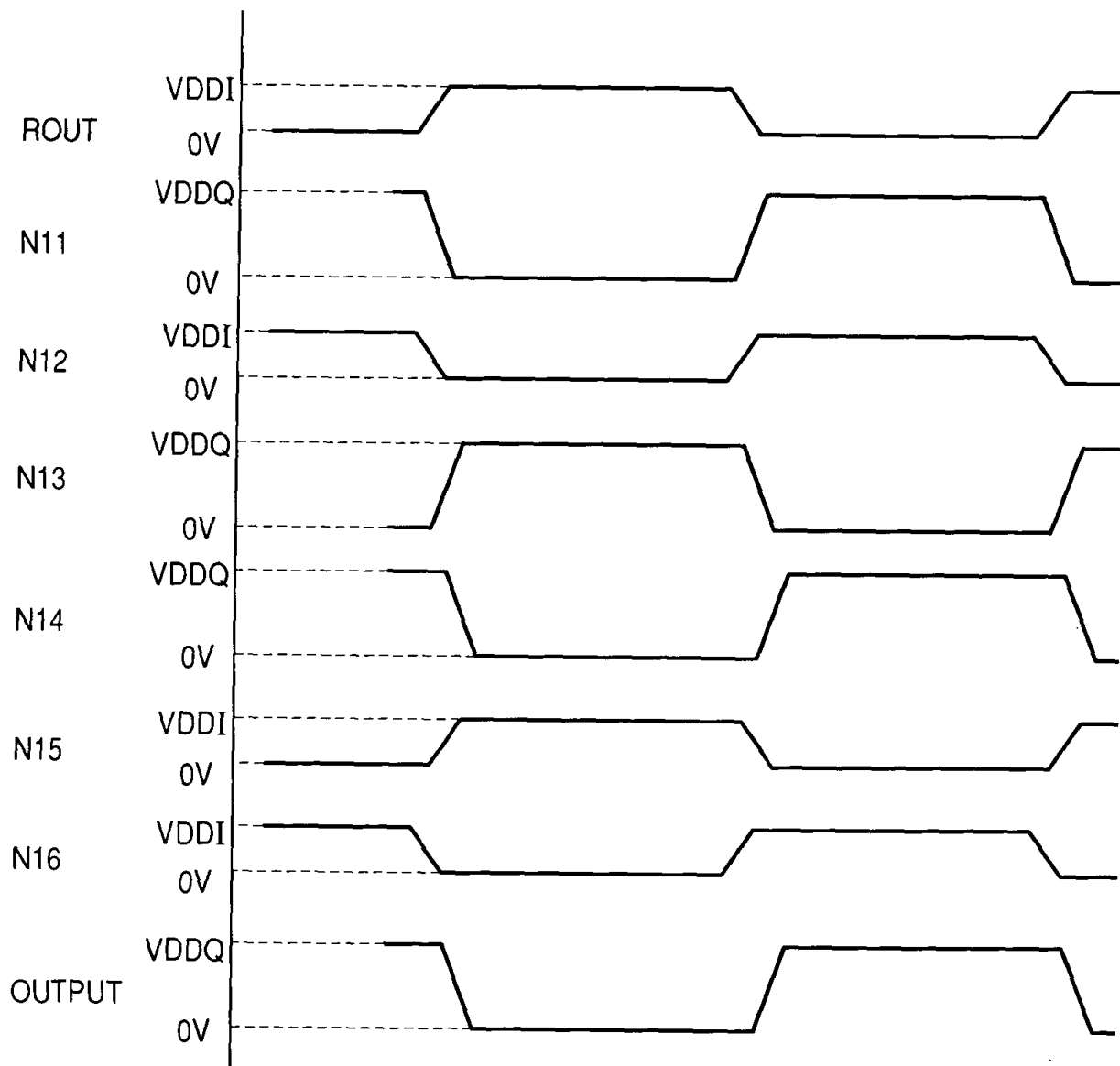


FIG. 5

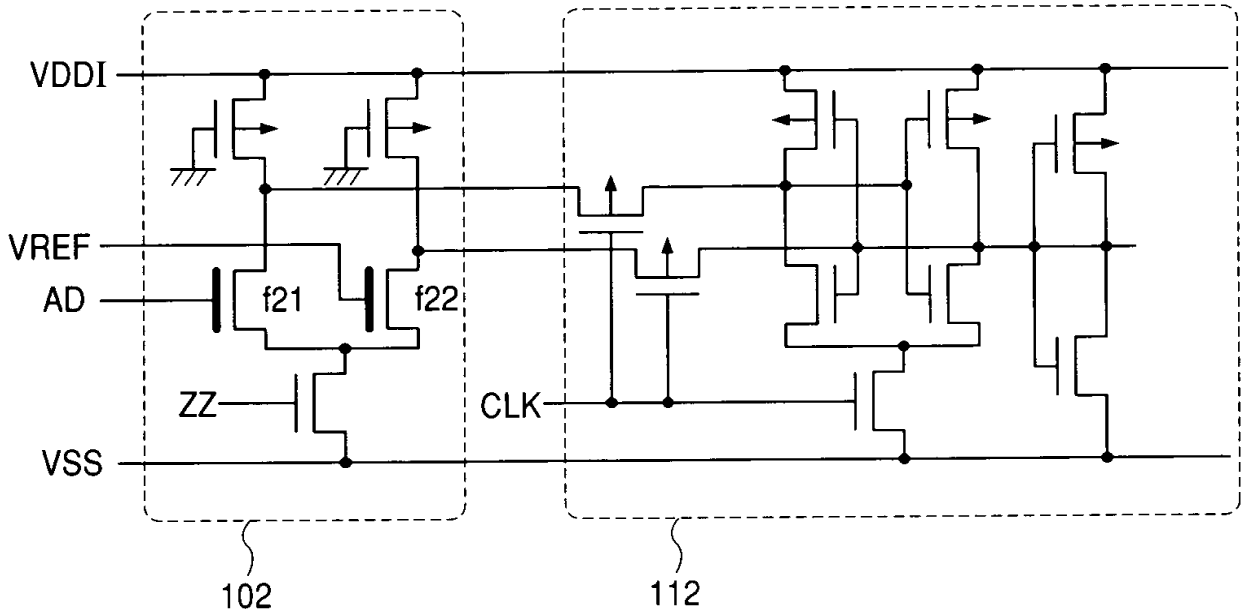


FIG. 6

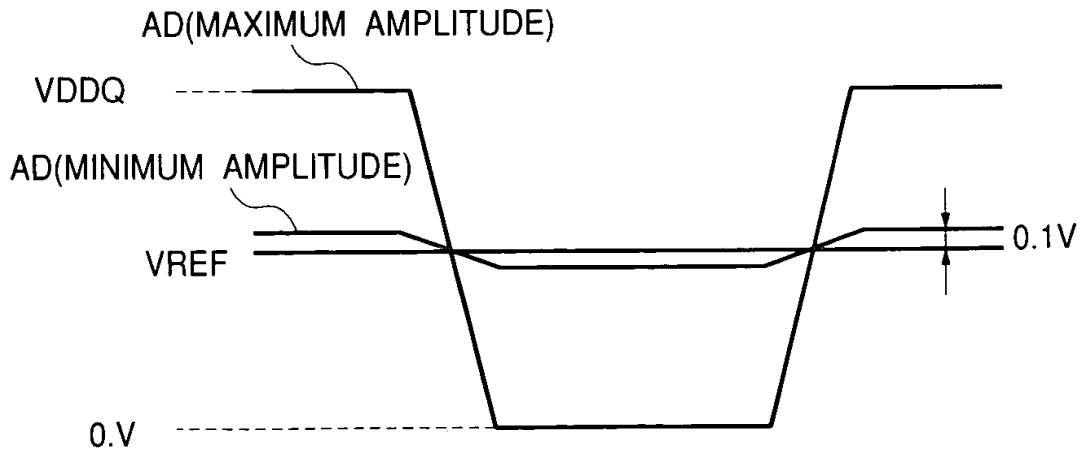
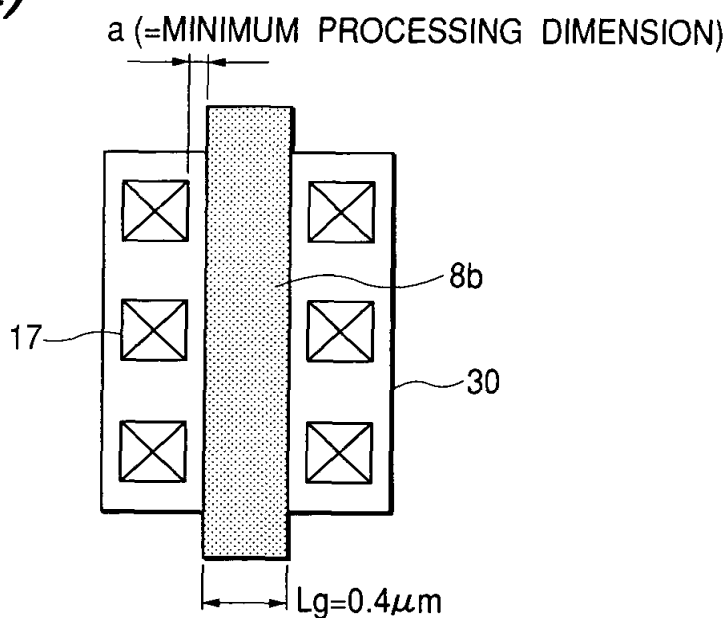
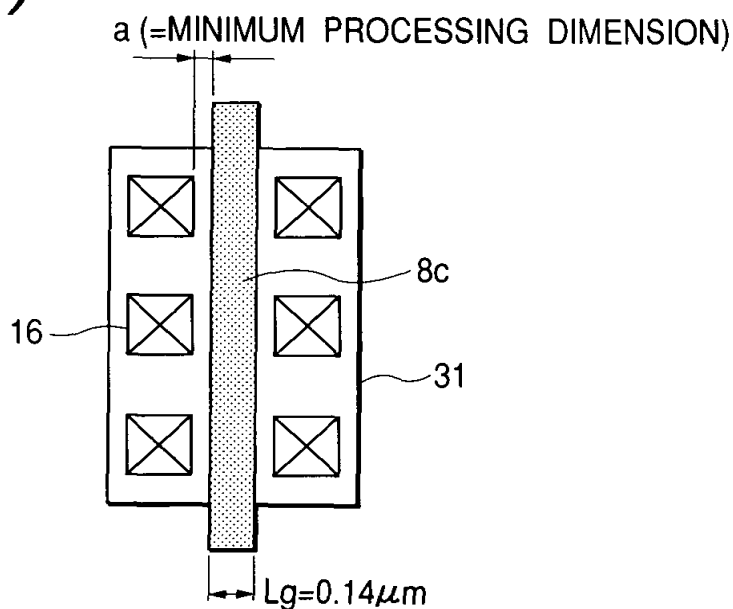


FIG. 7(a)



3.3V WITHSTANDING MOS TRANSISTOR

FIG. 7(b)



1.5V WITHSTANDING MOS TRANSISTOR

APPROVED	O.G. FIG.	
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FIG. 9

FIG. 9

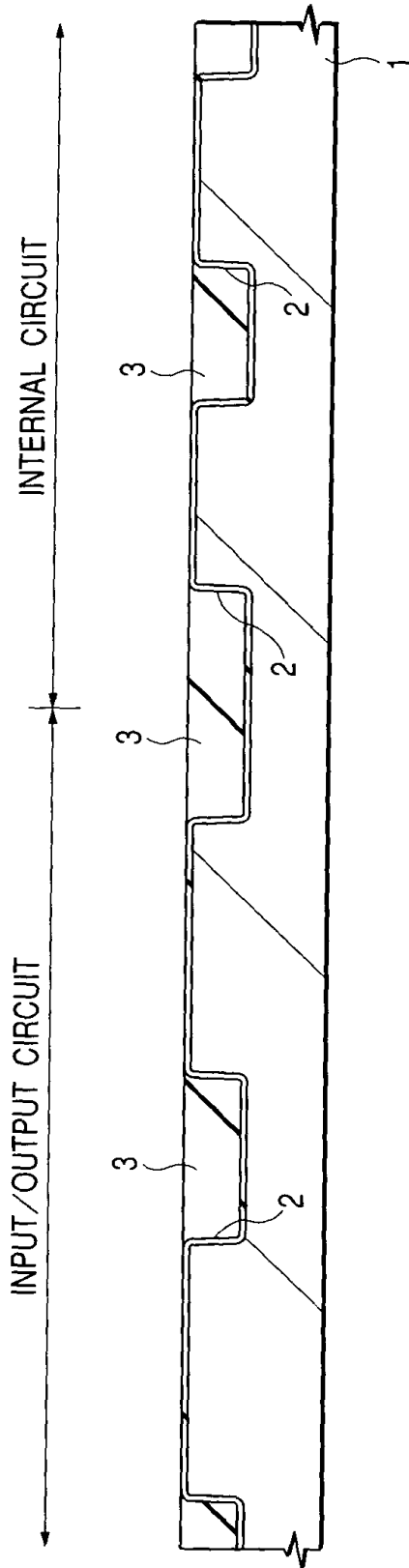
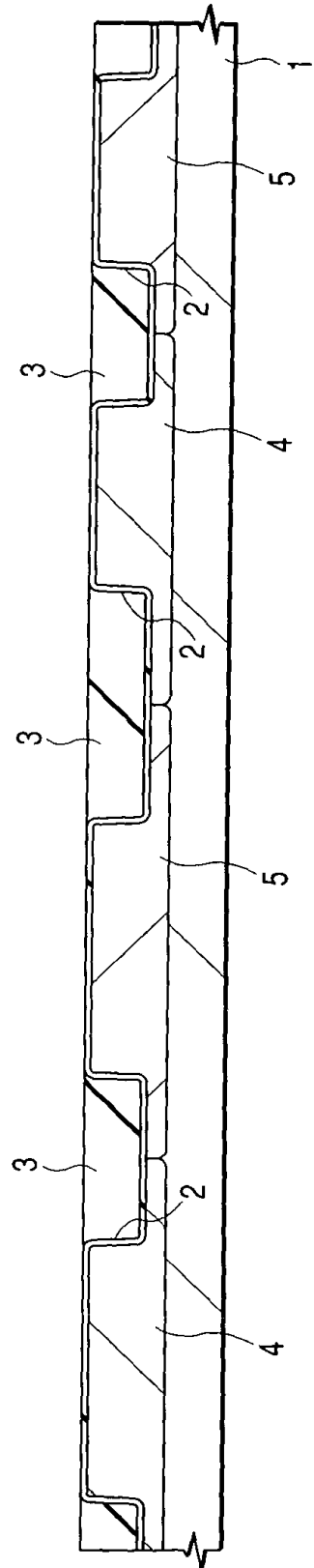


FIG. 10



APPROVED	O.G. FIG.
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FIG. 11(a)

FIG. 11(a)

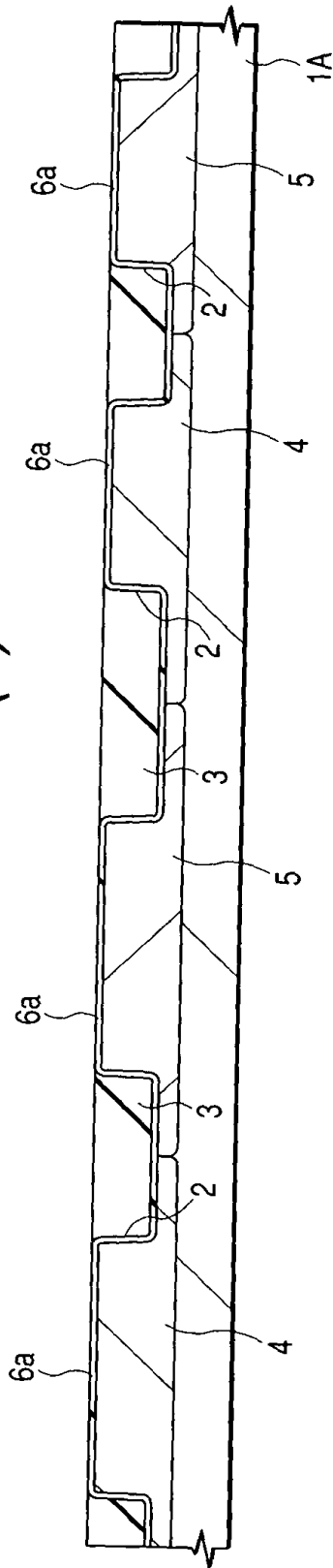
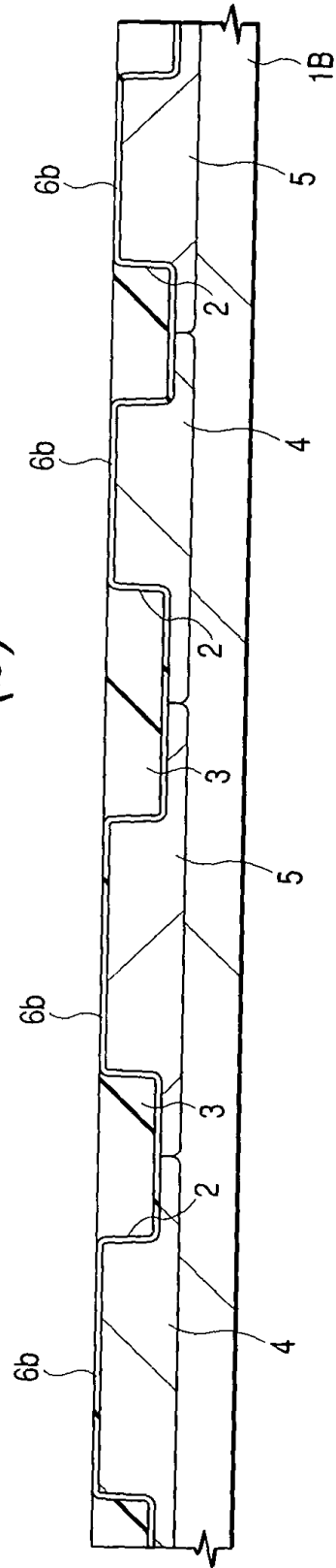


FIG. 11(b)



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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FIG. 12(a)

FIG. 12(a)

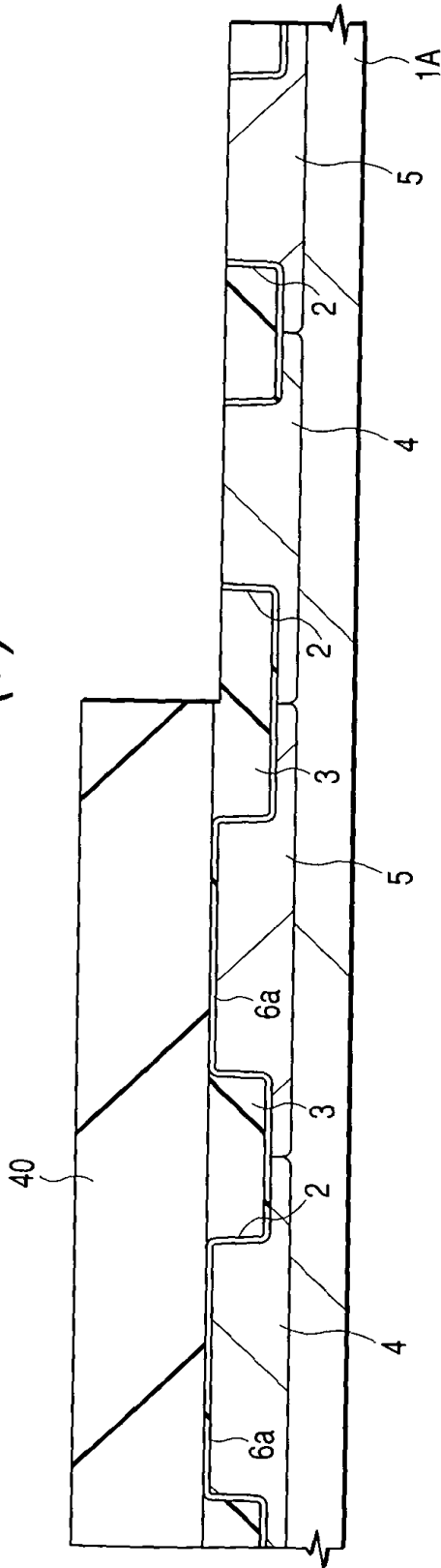


FIG. 12(b)

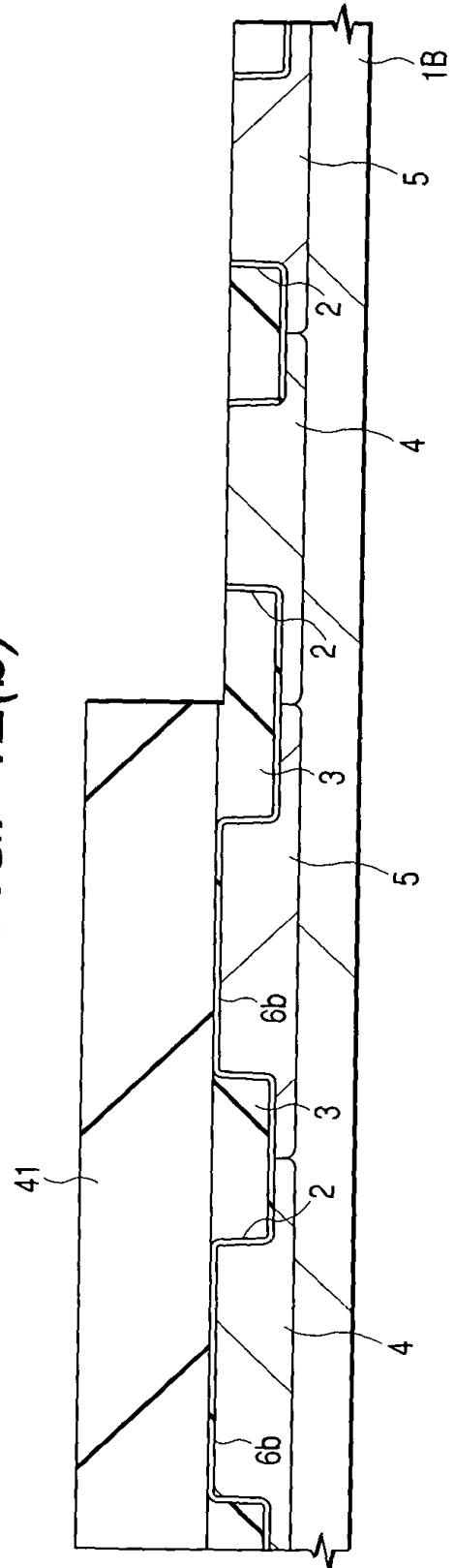


FIG. 13(a)

FIG. 13(a)

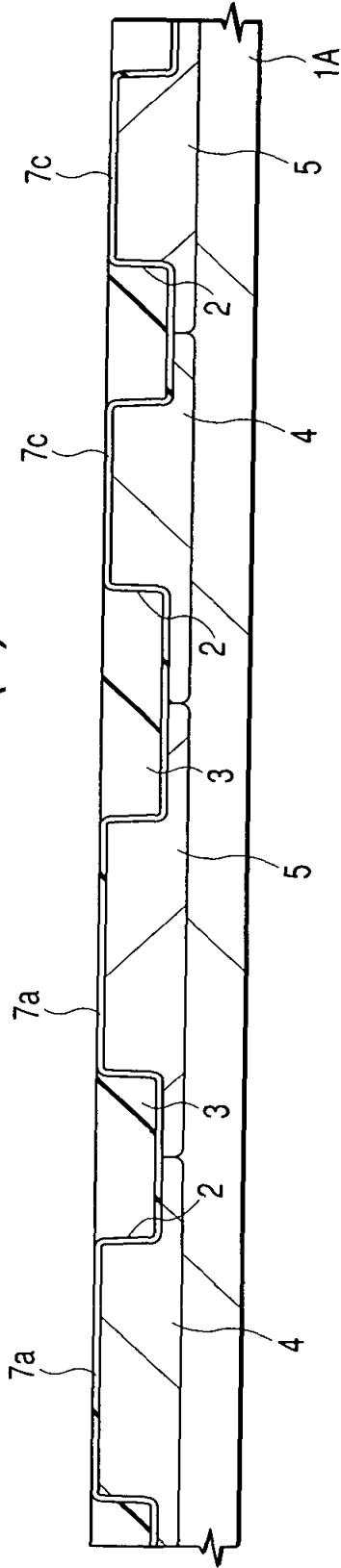
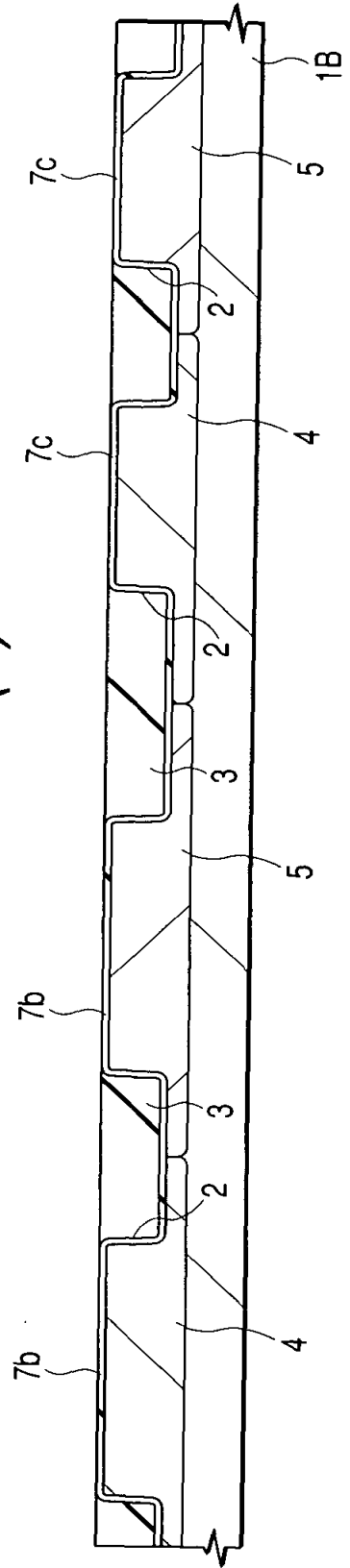


FIG. 13(b)



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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FIG. 14(a)

FIG. 14(a)

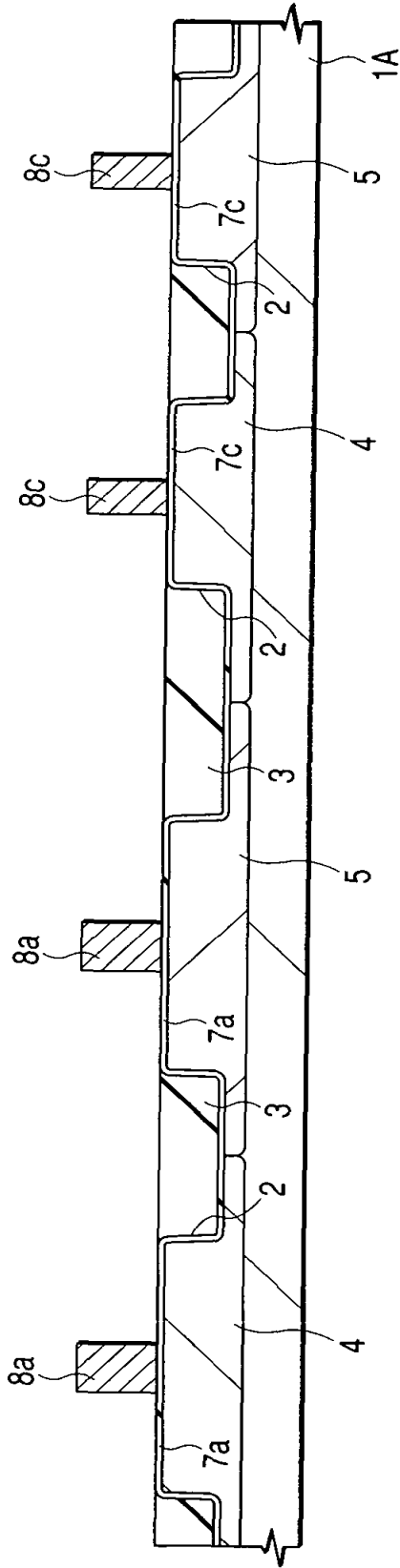
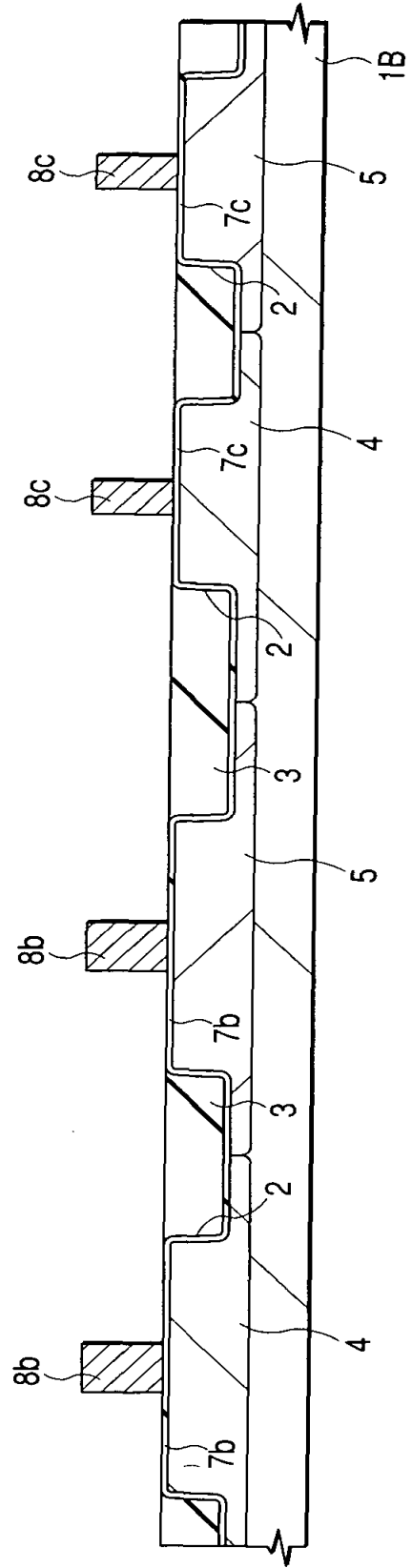


FIG. 14(b)



APPROVED	O.G. FIG.	
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TOP SECRET

FIG. 15(a)

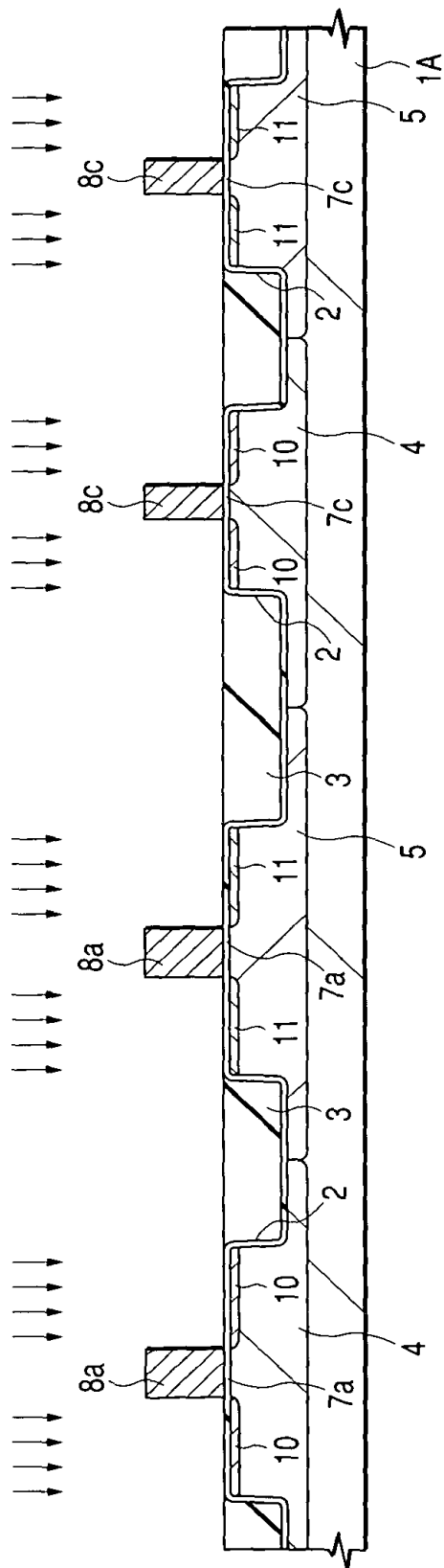


FIG. 15(b)

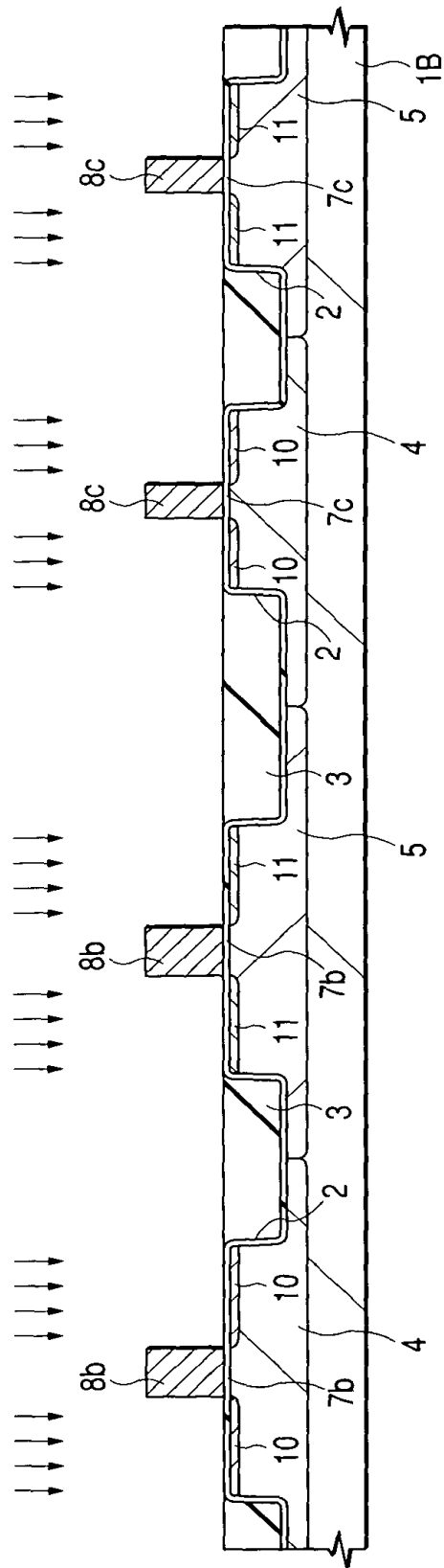


FIG. 16(a)

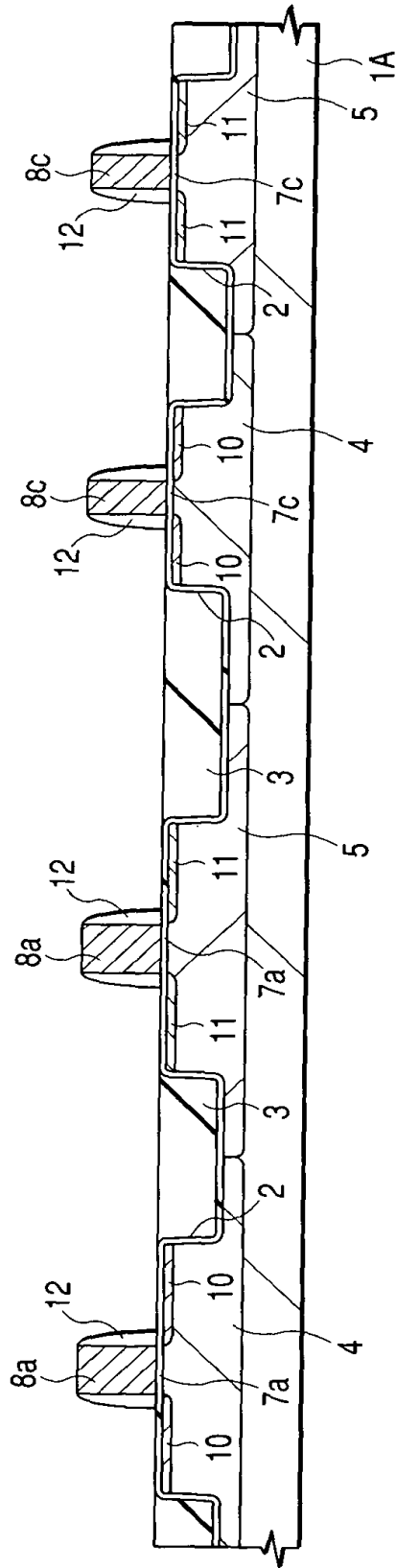
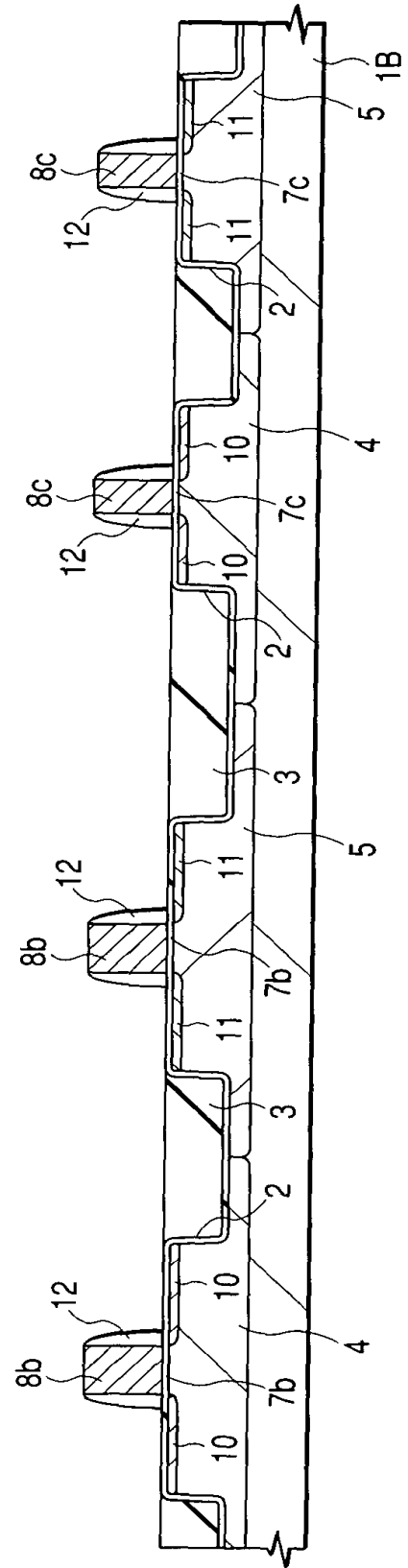


FIG. 16(b)



APPROVED	O.G. FIG.
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FIG. 18(a)

FIG. 18(a)

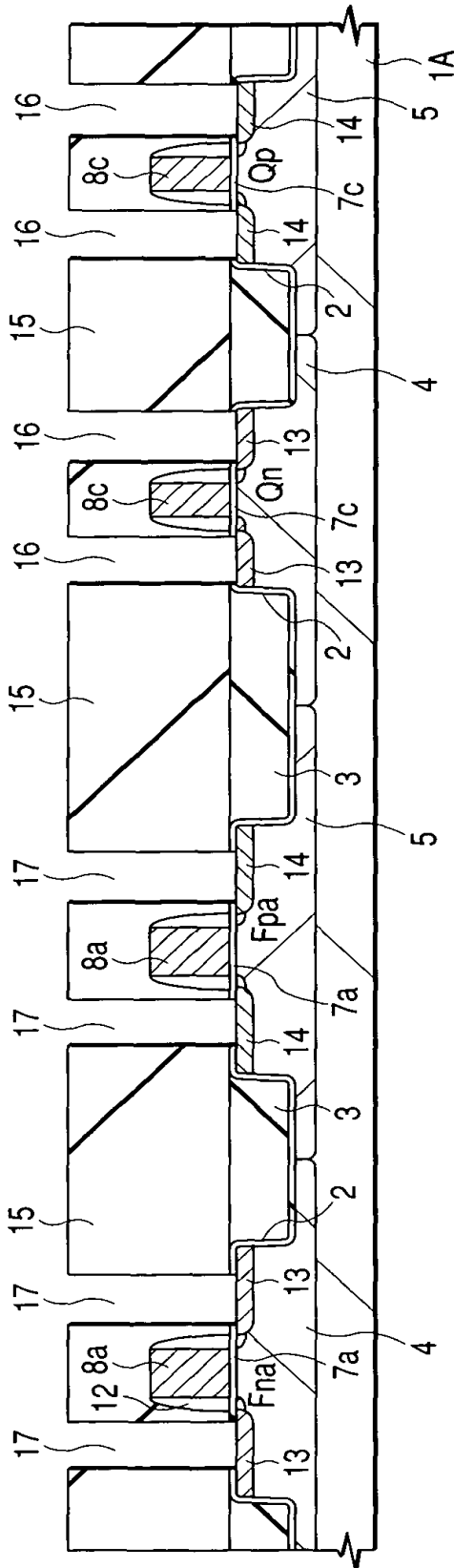


FIG. 18(b)

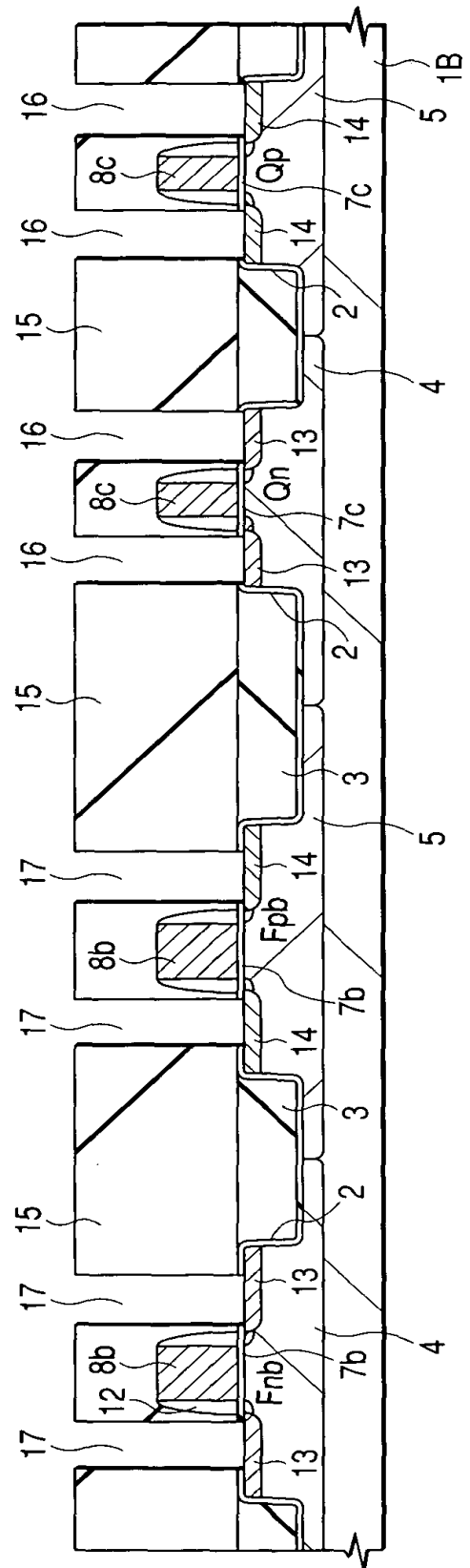
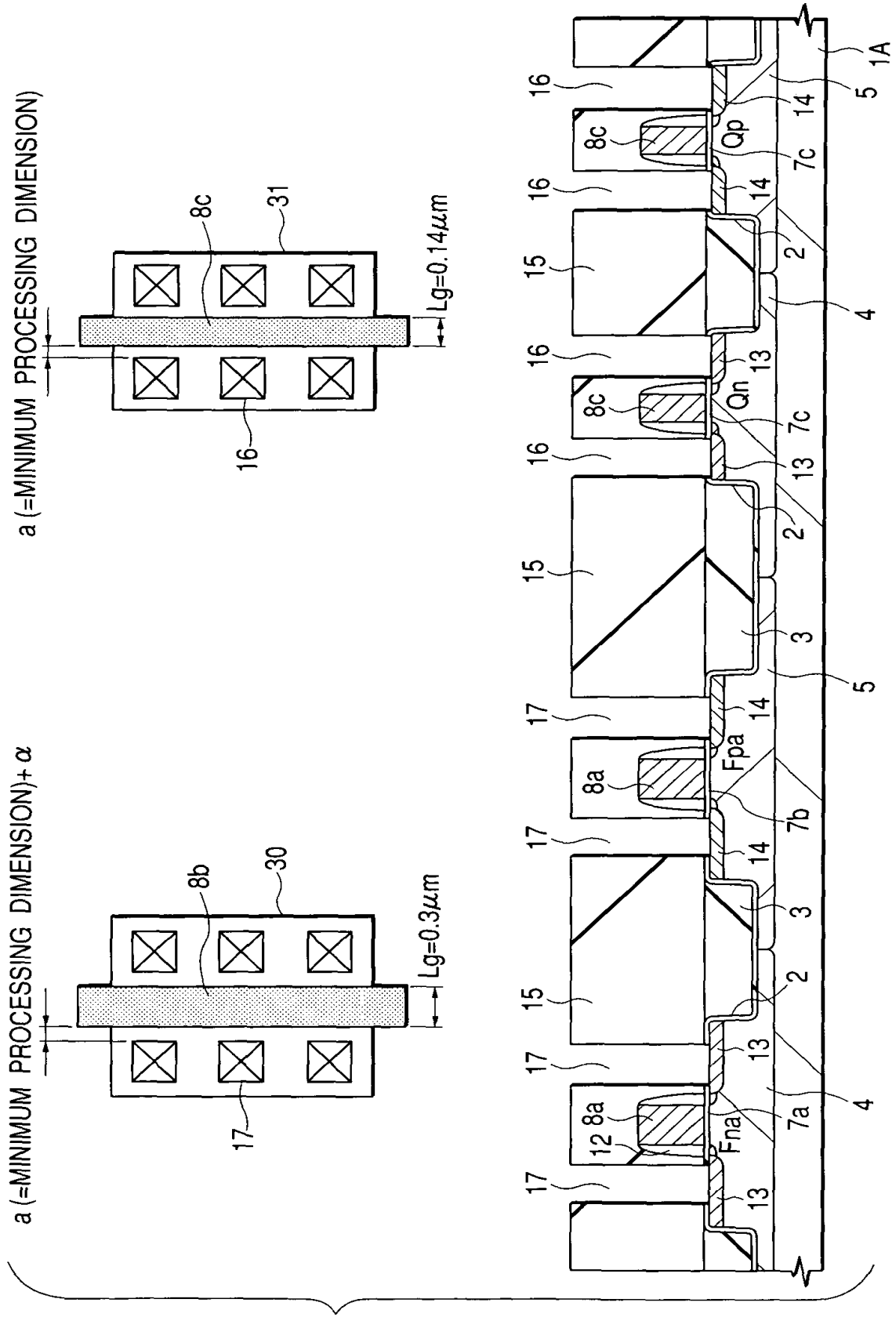


FIG. 20

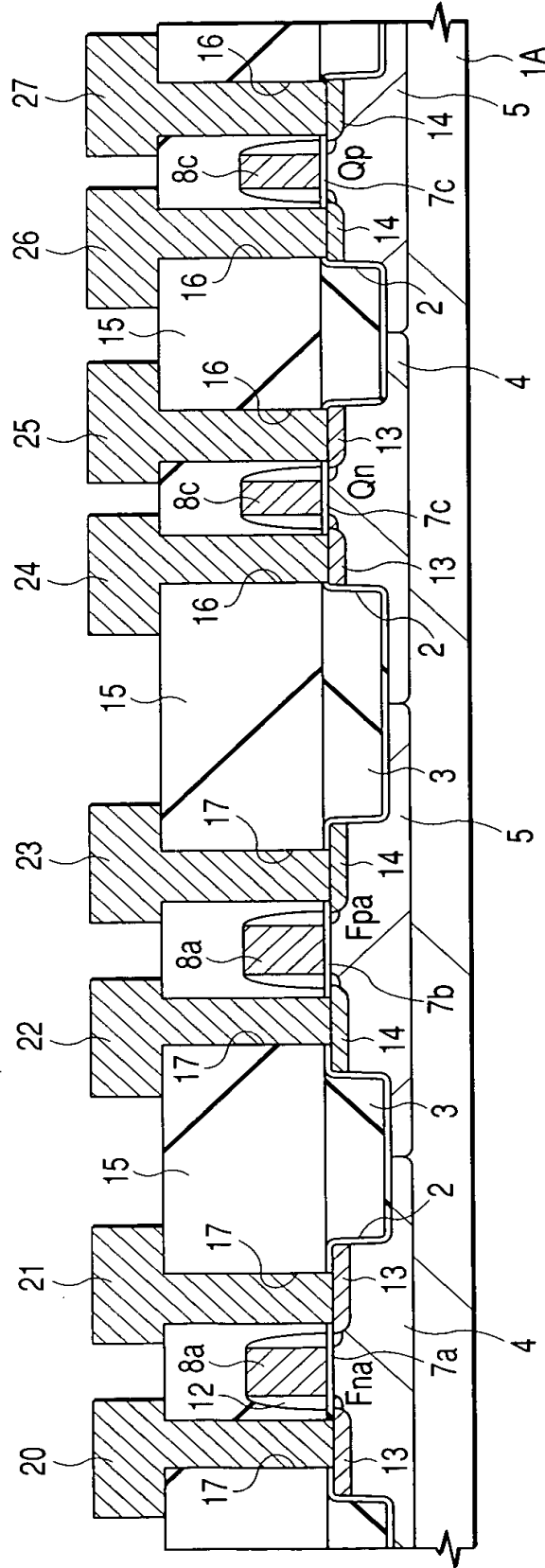


APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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FIG. 21

FIG. 21



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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FIG. 22

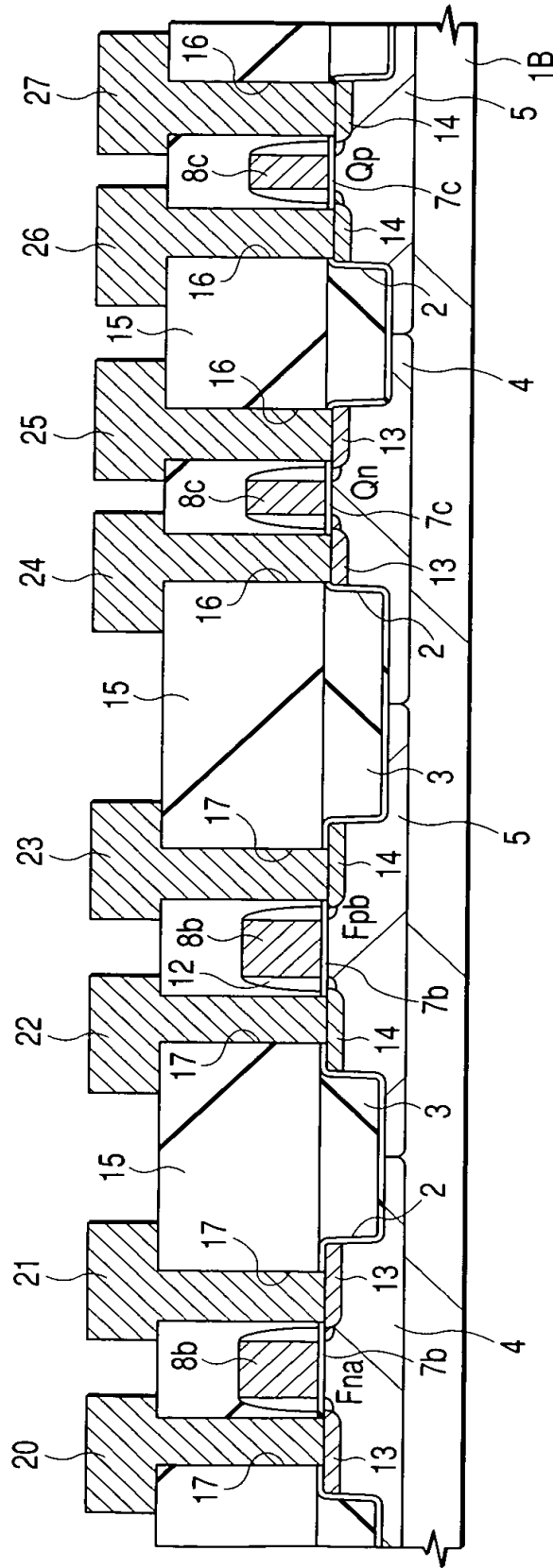


FIG. 23

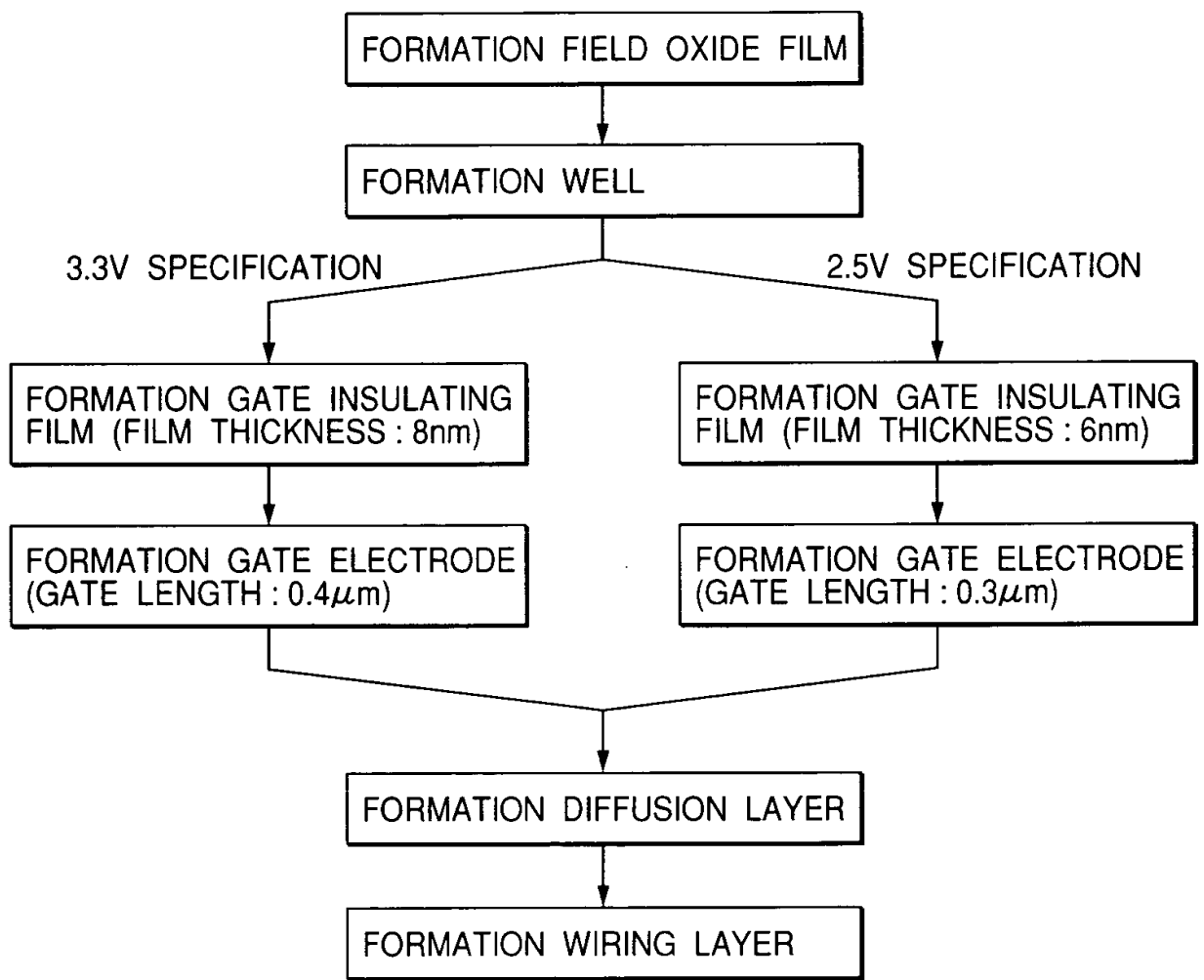


FIG. 23

FIG. 25

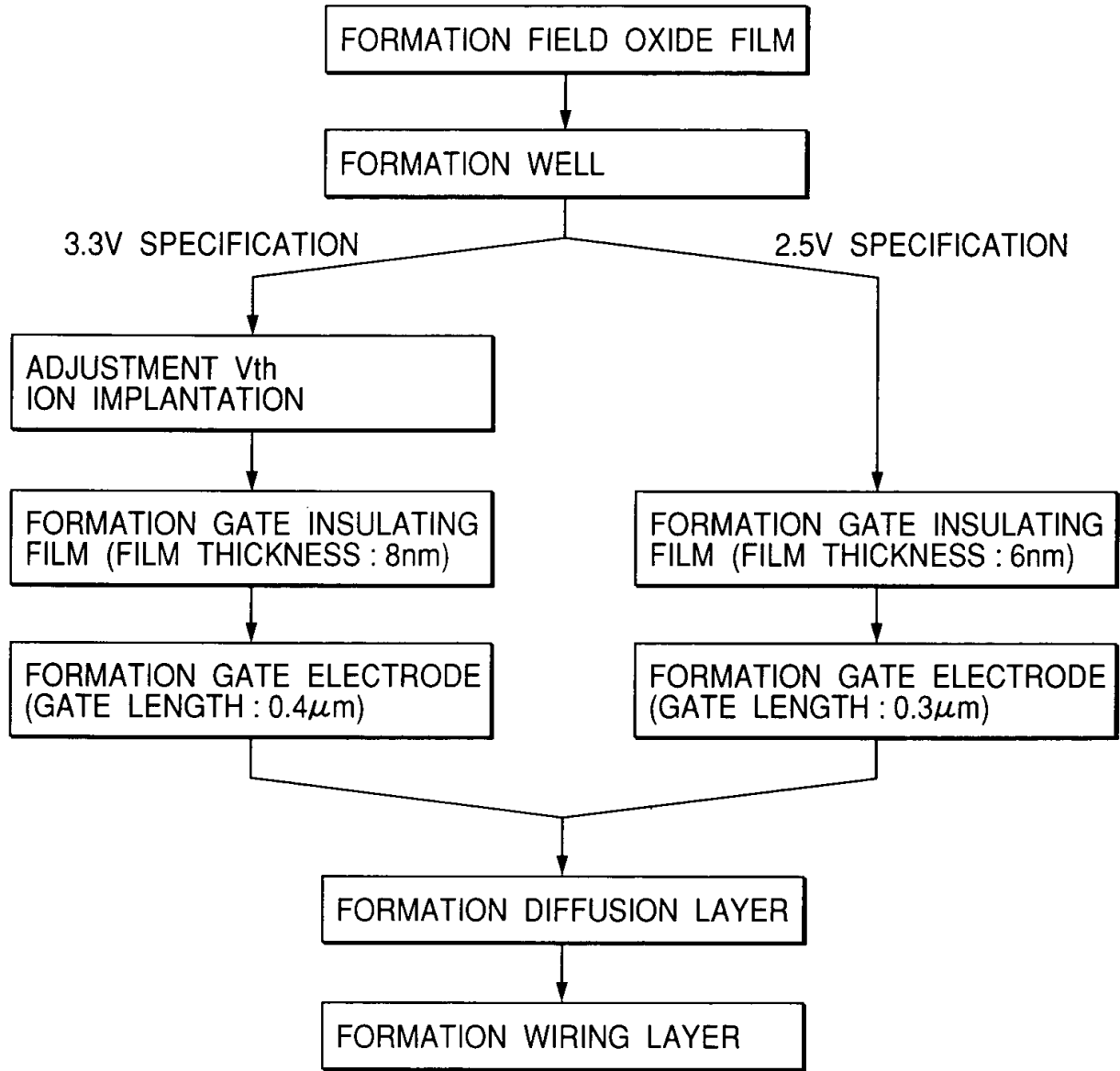
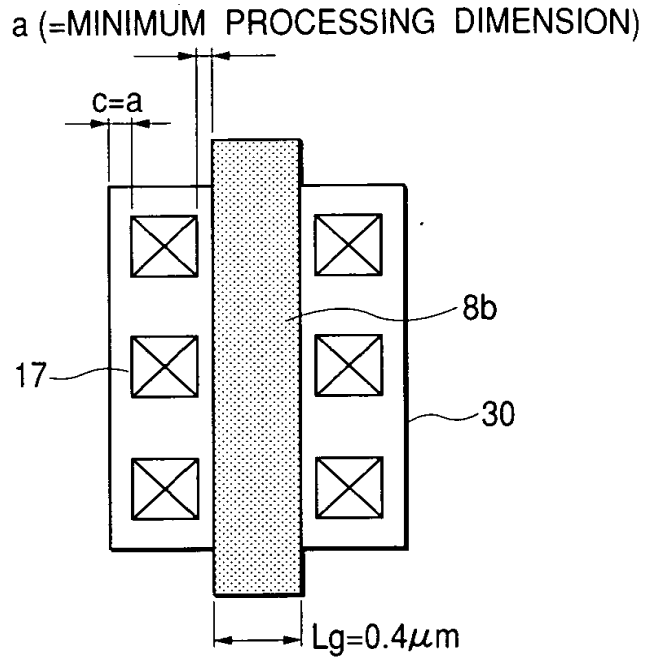
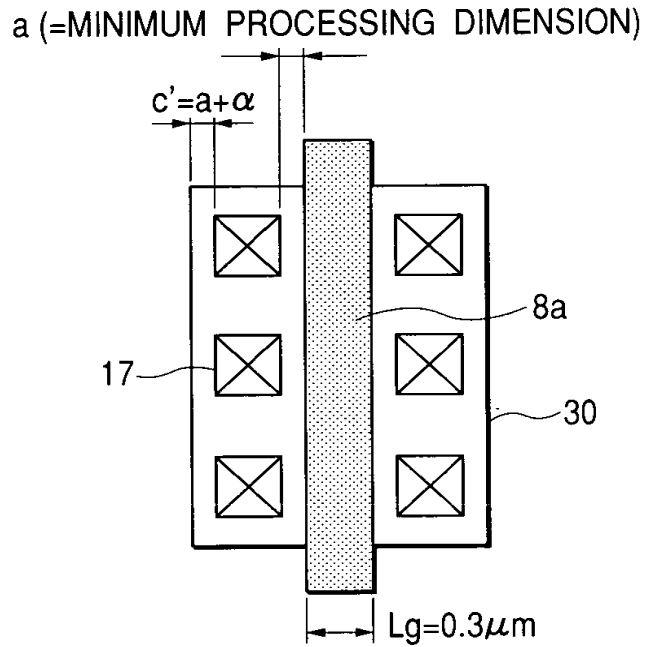


FIG. 25

FIG. 26



3.3V WITHSTANDING MOS TRANSISTOR



2.5V WITHSTANDING MOS TRANSISTOR

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 27

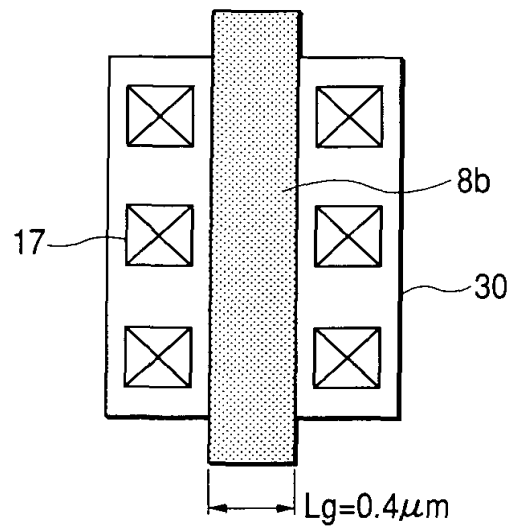
SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	1.5V	0V	VDDQ	1.5V

FIG. 27

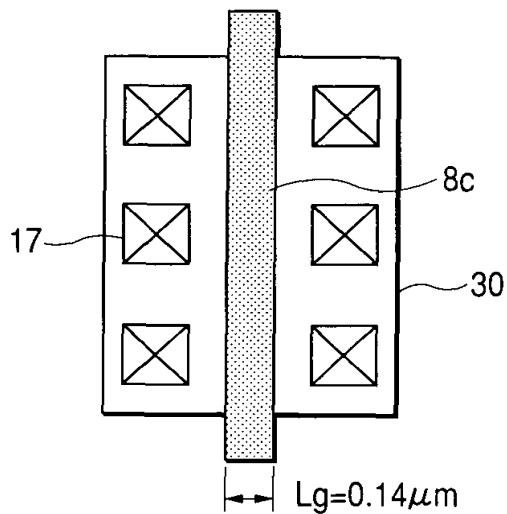
APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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FIG. 28



3.3V WITHSTANDING MOS TRANSISTOR



2.5V WITHSTANDING MOS TRANSISTOR

FIG. 28

FIG. 29

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	2.5V	0V	VDDQ	1.5V

FIG. 30

	GATE INSULATING FILM THICKNESS	MINIMUM PROCESSING GATE LENGTH
	TOX	Lg
3.3V WITHSTANDING MOS	8nm	0.4μm
2.5V WITHSTANDING MOS	6nm	0.3μm
1.5V WITHSTANDING MOS	3nm	0.14μm

FIG. 31

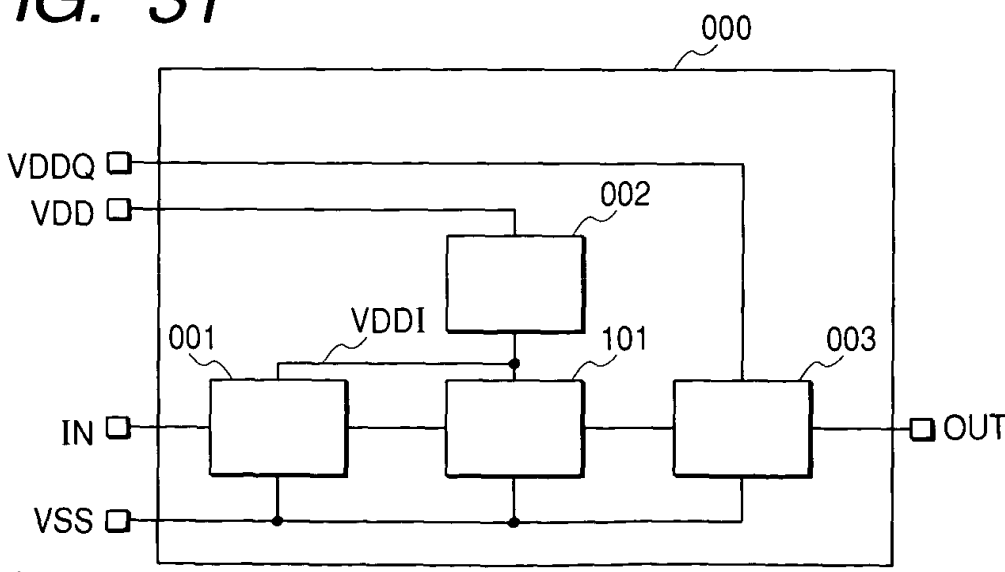
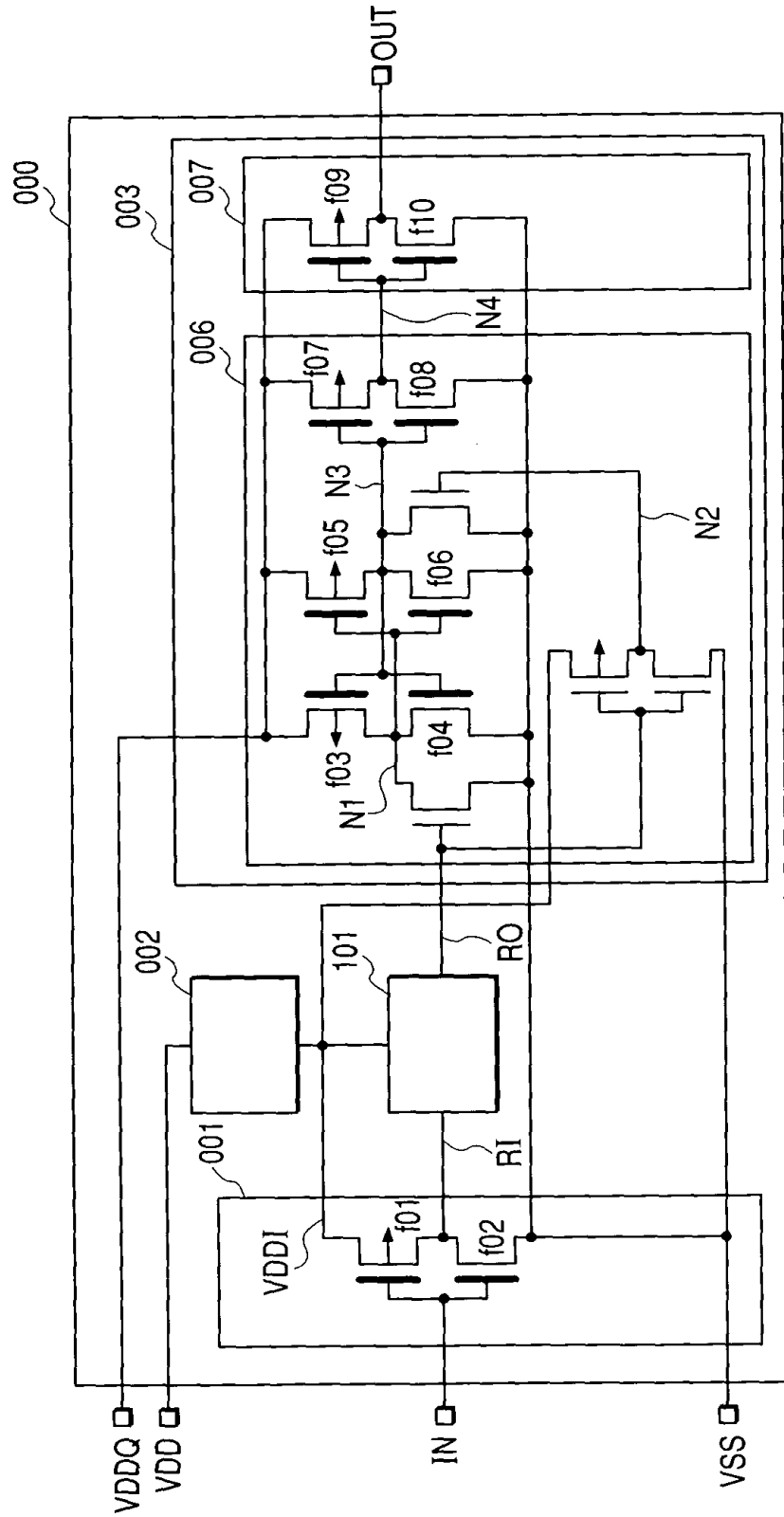


FIG. 32



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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FIG. 33

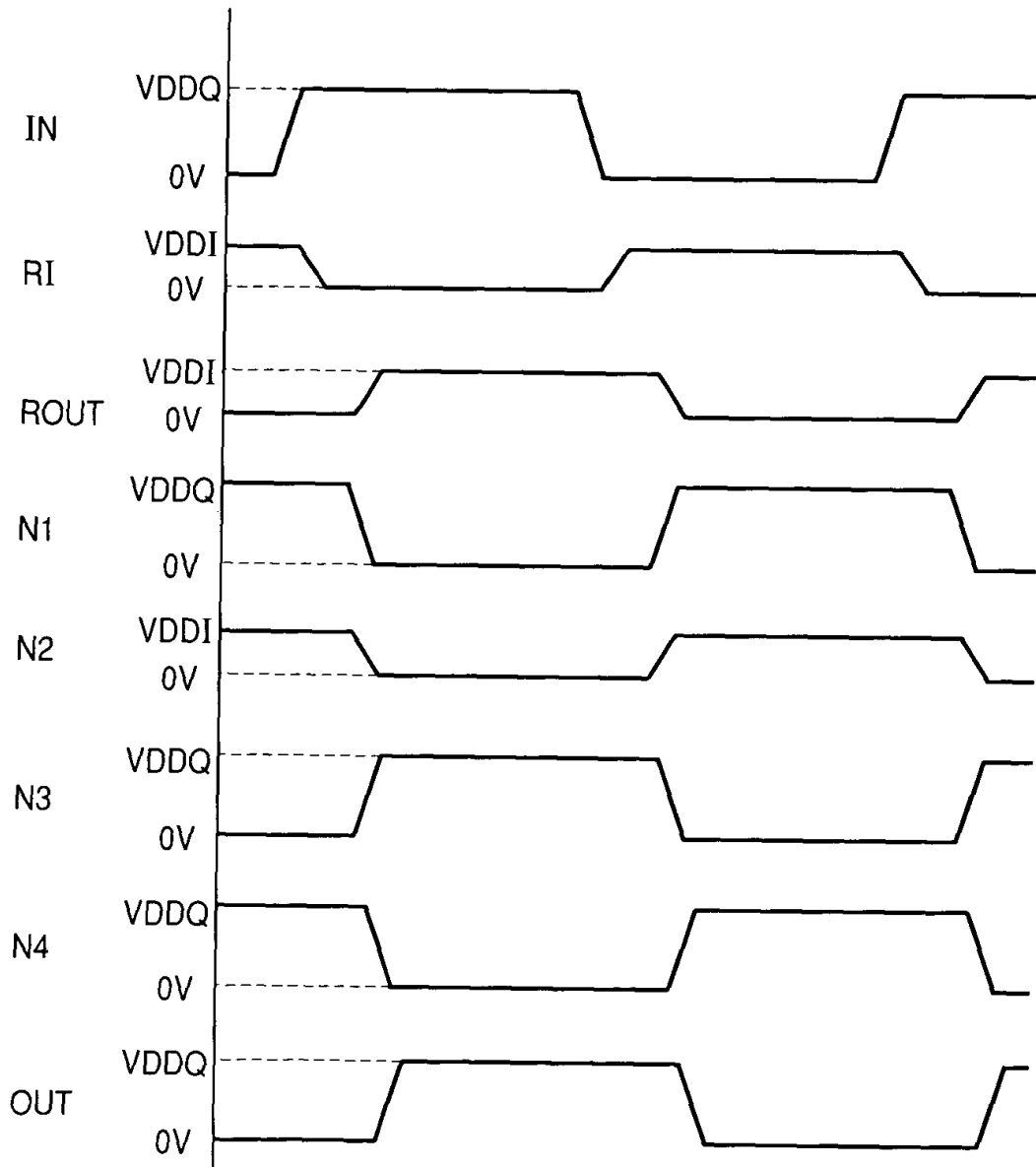


FIG. 33 = 6032000

FIG. 34

FIG. 34

